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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,184	02/02/2004	Kazuhiko Takahashi	OKI.638	3668

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VOLENTINE FRANCOS, & WHITT PLLC
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE SUITE 1260
RESTON, VA 20190

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,184	TAKAHASHI, KAZUHIKO	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-02-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. Applicant's Information Disclosure Statement, IDS, filed February 02, 2004 has been considered by the Examiner.

3. Claims 1 – 8 are pending.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Allen et al. (US Pat 6,560,137 B2).

Regarding **claims 1 and 7**, Allen et al. disclose a ferroelectric memory device (figs. 7 – 9), comprising:

a pair of bit lines including a first bit line and a second bit line (figs. 7 or 8, exemplary complementary pair of first bit line BL and second bit line BLb. The bit line pair BL/BLb corresponds to respective pairs BL0/BLb0, BL1/BLb1, BL2/BLb2, etc... in fig. 9);

a plurality of first 1T/1C memory cells each of which is connected to the first bit line (fig. 7 shows an exemplary pair of 1T/1C memory cells 24, in which the first cell, including M1 and CC1, is connected to bit line BL. Applicant please note that there are a plurality of the two memory cells 24 of fig. 7 shown connected in each of the respective bit line pairs in fig. 9, which make up the plurality of first 1T/1C memory cells);

a plurality of second 1T/1C memory cells each of which is connected to the second bit line (similarly, fig. 7 shows an exemplary second cell, including M2 and CC2, connected to bit line BLb. The plurality of cell pair 24 are connected in each respective bit line pairs of fig. 9 provide the plurality of second memory cells connected to the second bit line);

a plurality of word lines each of which is connected to a respective one of the first and second memory cells (figs. 7 and 9 show odd word lines WLO connected to the first memory cells and the even word lines WLE connected to the second memory cells. Both odd and even word lines provide the total N word lines of the memory array of fig. 9);

a plurality of plate lines each of which is commonly connected to respective pairs of the first and second memory cells (fig. 7 shows Common Plateline CP connected to capacitors CC1 and CC2 of the two memory cells 24. Similarly, fig. 14 shows common plateline CPL connected to both memory cell pair 28);

a plurality judgment memory cells (fig. 8, cell 26) each of which is connected between the first bit line and the second bit line (fig. 8, cell 26 connected to both bit lines BL and BLb), wherein each of the judgment memory cells includes tow transistors and two ferroelectric capacitors (fig. 8, cell 26 includes two transistors MR1 and MR2 and two capacitors CR1 and CR2. Further, common plateline CP also connected to both capacitors, similar to the configuration of fig. 7).

Regarding **claims 2 and 8**, Allen et al. also disclose the ferroelectric memory devices of claims 1 and 7, further comprising a plurality of judgment word line pairs (figs. 8 and 9, WRE and WRO) each of which is connected to a respective one of the judgment memory cell (col. 3, line 66 – col. 4, line 19), and wherein the judgment word lines of each judgment word line pair are supplied with a common voltage level (figs. 20, 22, and 24 show the same voltage level, VCC, supplied to WL0 and WRE during logic high. Similarly, fig. 3 shows Vcc supplied to word line WL for logic high).

Regarding **claim 3**, Allen et al. also disclose the ferroelectric memory device of claim 1, further comprising a plurality of judgment word line pairs and a plurality judgment plate lines each connected to respective ones of the judgment

memory cells (fig. 25 show a comprehensive array with at least two reference cells REF CELL over each bit line pair. Therefore, with the possibility of two of cells 26 of fig. 8 in place of each these REF CELL, a plurality of judgment word line pairs WRO0/WRE0 and WRO1/WRE1, and common plate lines CP0, CP1, etc... are provided).

Regarding **claim 4**, Allen et al. also disclose the ferroelectric memory device of claim 1, wherein each of the judgment memory cell includes:

a fist transistor (fig. 8, MR1) which has a gate electrode connected to one judgment word line (fig. 8, gate electrode of MR1 connected to WRO) of a respective judgment word line pair, a first electrode connected to the first bit line (fig. 8, one electrode of MR1 connected to bit line BL) and a second electrode;

a first capacitor connected between a respective judgment plate line and the second electrode of the first transistor (fig. 8, CR1 connected between the other electrode of transistor MR1 and plateline CP);

a second transistor which has a gate electrode connected to the other judgment word line of the respective judgment word line pairs (fig. 8, second transistor MR2, whose gate is connected to WRE), a first electrode connected to the second bit line (fig. 8, the gate electrode of MR2 which connects to bit line BLb);

a second ferroelectric capacitor connected between the judgment plateline and the second electrode of the second transistor (fig. 8, CR2 connected between the other electrode of transistor MR2 and plateline CP).

Regarding **claim 5**, Allen et al. also disclose the ferroelectric memory device of claim 4, wherein each of the first memory cells includes a third transistor (fig. 7, transistor M1) which has a gate electrode connected to a respective word line (fig. 7, word line WLO), a first electrode connected to the first bit line (fig. 7, first electrode connected to bit line BL) and a second electrode, and a third capacitor connected between a respective plateline and the second electrode of the third transistor (fig. 7, capacitor CC1 connected between transistor M1's second electrode and plateline CP), and wherein each of the second memory cells includes a fourth transistor (fig. 7, transistor M2) which has a gate electrode connected to a respective word line (fig. 7, the gate connected to WLE), a first electrode connected to the second bit line (fig. 7, the electrode connected to the bit line BLb) and a second electrode, and a fourth capacitor connected between the respective plate line and the second electrode of the fourth transistor (fig. 7, capacitor CC2 connected between transistor's M2's second electrode and plate line CP).

Regarding **claim 6**, Allen et al. also disclose the ferroelectric memory device of claim 1, further comprising a plurality of digit line pairs (fig. 37, input/output pairs IO0/IOb0, IO1/IOb1, etc...) and a plurality of gate transistor pairs (fig. 37, transistor pairs m1s2/m2s2, m3s2/m4s2, etc... which connect to the corresponding input/output pairs), wherein each of the gate transistor pairs connects a sense amplifier to a respective digit line pair (figs. 36 and 37 show these transistors opening or closing the connections between the input/output line pairs to their respective bit line pairs, whose signals are coming from

respective sense amplifiers SA0, SA1, SA2, etc..., as shown in figs. 9, 18, 25, 26, 35).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3 – 5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirano et al. (US Pat 5,751,628).

Regarding **claims 1, 3 – 5, and 7**, Hirano et al. disclose a ferroelectric memory device (fig. 1, col. 3, line 10 – col. 6, line 55), comprising:

a first bit line (bit line BL);

a second bit line (bit line /BL);

a plurality of first memory cells each of which is connected to the first bit line, wherein each of the first memory cells includes one transistor and one ferroelectric capacitor (memory cells connected to bit line BL including Qn0 and C0, Qn2 and C2, etc... to the 255th cell including Qn254 and C254);

a plurality of second memory cells each of which is connected to the second bit line, wherein each of the second memory cells includes one transistor and one ferroelectric capacitor (memory cells connected to bit line /BL including Qn1 and C1, Qn3 and C3, etc... to the 256th cell including Qn255 and C255);

plurality of word lines each of which is connected to a respective one of the first and second memory cells (word lines WL0, WL2, WL4, etc... are connected to the first plurality of memory cells, wherein word lines WL1, WL3, WL5, etc... are connected to the second plurality of memory cells);

a plurality of plate lines each of which is commonly connected respective pairs of the first and second memory cells (for each bit line pairs BL and /BL, there is a plate line commonly connected to the first memory cells and the second memory cells. As a result, there would be N number of plate lines for a corresponding N bits of the array);

a plurality of judgment memory cells each of which is connected between the first bit line and the second bit line, wherein each of the judgment memory cells includes two transistors and two ferroelectric capacitors (reference cells including transistor/capacitor QnD0/DC0 and QnD1/DC1, respectively connected to reference word lines DWL0 and DWL1, for each bit line pair).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
October 4, 2005

HUAN HOANG
PRIMARY EXAMINER